1 SPI NAND Flash Memory

1.1 Features

OTP SIZE

- 8K-Byte OTP

Standard, Dual, Quad SPI

- Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
- Dual SPI: SCLK, CS#, SIO0, SIO1, WP#, HOLD#
- Quad SPI: SCLK, CS#, SIO0, SIO1, SIO2, SIO3

SPI Clock Frequency

- 104Mbits/s

Programmable ECC

- 4-14 bit ECC

Electrical Characteristics

- input voltage: 2.7~3.6V

Operating Temperature

- Commercial：-40℃~85℃

1.2 Product Information

Table 1-2 Product Information

Part Number	Density	Page Size	Block Size	Mid	DID	Package
HX25Q1GASLCG	128MB	(2K + 64) Byte	(128K + 4K) Byte	ECh	F1h	WSON

2 SPI NAND PIN Assignment

2.1 SPI PIN

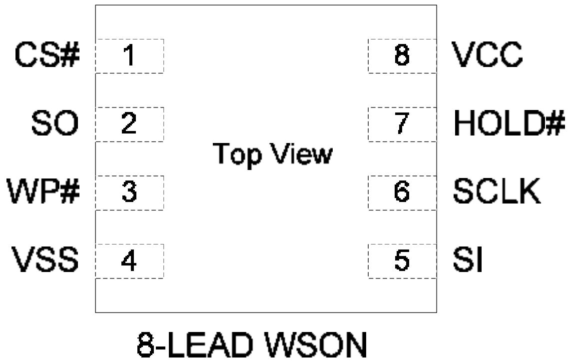


Figure 2-1 SPI NAND Flash Memory

2.2 PIN Description

Table 2-1 SPI Flash Memory PIN Description

Pin Name	I/O	Description
CS#	I	Device selection, active low
SO/SIO1	I/O	Serial data output /serial data bidirectional IO (SIO1)
WP#/SIO2	I/O	Write protection, active low / serial data bidirectional IO (SIO2)
VSS	Ground	Ground
SI/SIO0	I/O	Serial data input /serial data bidirectional IO (SIO0)
SCLK	I	Serial clock
HOLD#/SIO3	I/O	Hold enable, active low, serial data bidirectional IO (SIO3)
VCC	Supply	Power Supply

2.3 Block Diagram

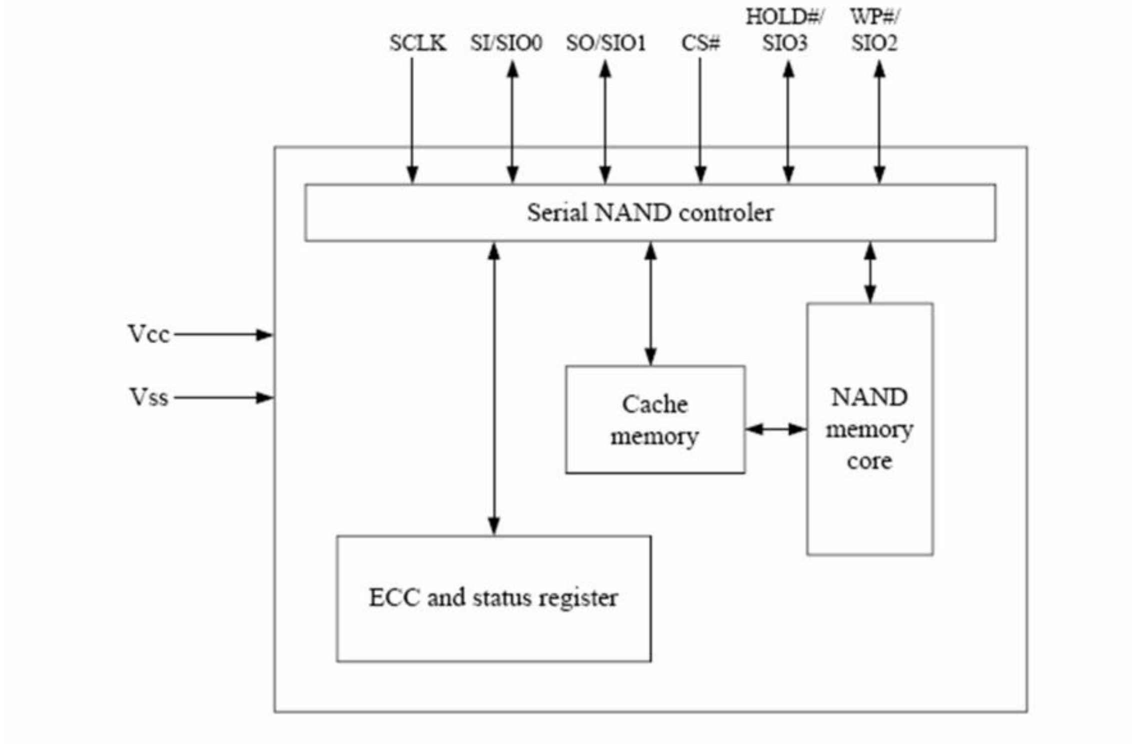
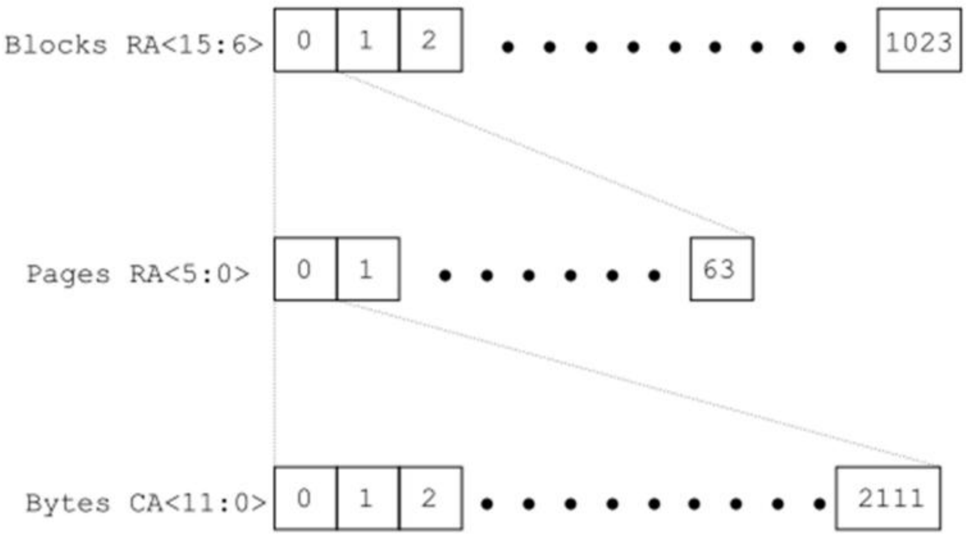


Figure 2-2 Block Diagram of SPI NAND Flash Memory

2.4 Memory Mapping Diagram



Notes:

1.CA:Column Address.The 12-bit address is capable of addressing from 0 to 4095 bytes;
however,only bytes 0 through 2111 are valid.
Bytes 2112 through 4095 of each page are "out of bounds,"
do not exist in the device and can not be addressed.

2.RA:Row Address.RA<5:0> selects a page inside a block and RA<15:6> selects a block.

Note:page size = 2048 Bytes, spare size = 64 Bytes

3 SPI NAND Operation

3.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 （Mode 0）
- CPOL = 1, CPHA = 1 （Mode 3）

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode. See Figure 4-1 The timing diagrams shown in this data sheet are mode 0.

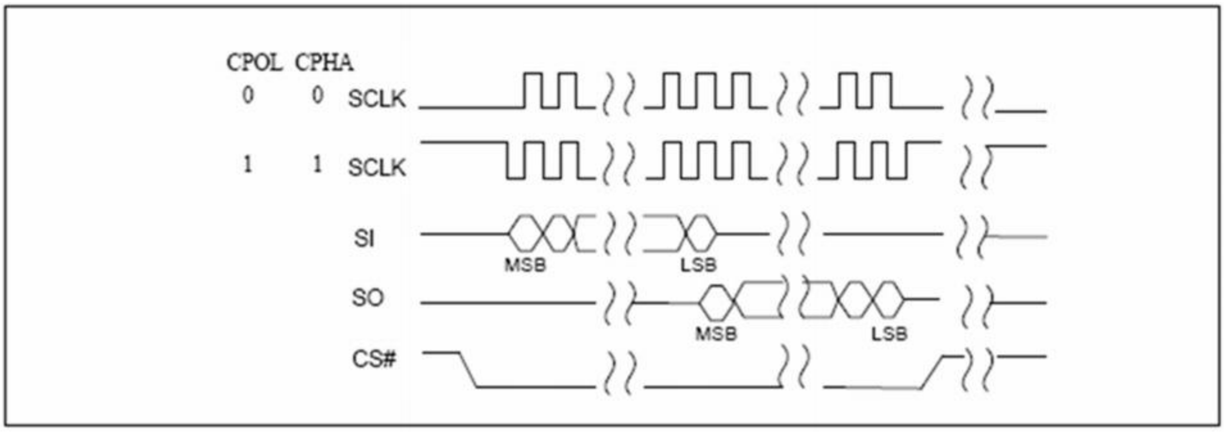


Figure 3-1 SPI Timing Diagram of SPI Modes

Standard SPI

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out (SO)

Dual SPI

The device supports dual SPI operation with x2 and dual IO commands. These commands allow data to be transferred to or from the device at two times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1.

Quad SPI

The device supports the x4 and Quad commands operation. These commands allow data to be transferred to or from the device at four times of rates of Standard SPI operation. The SI and the SO become bi-directional I/O pins: SIO0 and SIO1. The WP# and the HOLD# pins become SIO2 and SIO3.

3.2 Hold Mode

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of writing status register, programming or erasing in progress.

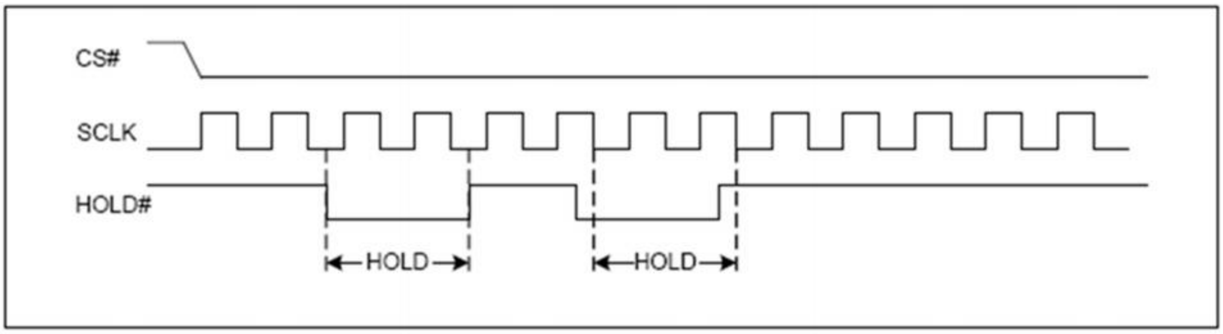


Figure 3-2 HOLD condition Diagram

Note:

Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. When SCLK is HIGH and HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

3.3 Write Protection Mode

Write protect (WP#) provides hardware protection mode. The WP# prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can not be altered.

4 SPI NAND Command Set

Table 5-1 commands Set

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	ByteN
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			Wrap
Set Feature	1FH	A7-A0	(D7-D0)	Dummy		
Page Read(to cache)	13H	A23-A16	A15-A8	A7-A0		
Read form Cache	03H/0BH	A15-A8	A7-A0	dummy	(D7-D0)	Wrap
Read form Cache x 2	3BH	A15-A8	A7-A0	dummy	(D7-D0)x2	Wrap
Read form Cache x 4	6BH	A15-A8	A7-A0	dummy	(D7-D0)x4	Wrap
Read form Cache Dual IO	BBH	A15-A0	dummy	(D7-D0)x2		Wrap
Read form Cache Quad IO	EBH	A15-A0	(D7-D0)x4			Wrap
Read ID	9FH	A7-A0	MID	DID		Wrap
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load x 4	32H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load random data	84H	A15-A8	A7-A0	(D7-D0)	Next byte	Byte N
Program Load random data x 4	C4H/34H	A15-A8	A7-A0	(D7-D0)x4	Next byte	Byte N
Program Load random data Quad IO	72H	A15-A0	(D7-D0)x4	Next byte		Byte N
Block Erase	D8H	A23-A16	A15-A8	A7-A0		
Reset	FFH					

5 SPI NAND Command Operation

5.1 RESET Operation - Reset（FFH）

The RESET (FFH) command stops program, write and erase operations.

When RESET (FFH) command is operating, OIP is set to 1. Use GET FEATURE (0FH) command to check the OIP bit. If OIP = 0, the reset operation is finished. Users then can access SPI NAND FLASH.

P_FAIL, E_FAIL, WEL, ECCS1, and ECCS0 will be reset after the Reset (FFH) command is received.

(Optional) The data of Block 0 Page 0 will be automatically loaded to cache after the RESET (FFH) command is received, and ECCS1 and ECCS0 will show BCH results.

The command sequence is described as follows:

- FFH （RESET）
- 0FH （GET FEATURE）

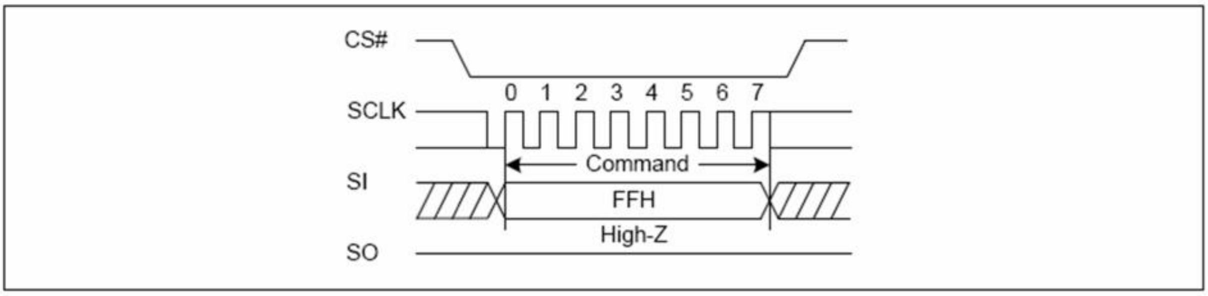


Figure 6-1 Reset Sequence Diagram

Notes:

1. Users should use RESET (FFH) command and GET FEATURE (0FH) command after power-up to confirm that the system is initialized (Block 0 Page 0 are loaded; the internal initialization finished). Otherwise, premature command accessing will lead to some unexpected results. If not to use the RESET (FFH) command, the device should not be operated until 5ms past power-up.

2. Users should use the GET FEATURE (0FH) command after using the RESET (FFH) command to make sure that the interrupt operation is completed (OIP = 0) and finish the loading of Block 0 Page 0. Otherwise, it will result in some unexpected results.

5.2 Read ID（9FH）

The READ ID command is used to identify the SPI NAND FLASH and reads a two-byte table that includes the Manufacturer ID and Device ID. Table 6-1 shows the address and description of the register. Table 5-2 shows the command sequence.。

Table 6-1 READ ID Table

Address	Value	Description
00H	-	Manufacturer ID（ApDevice）
01H	-	Device ID（1Gb/2Gb/4Gb）

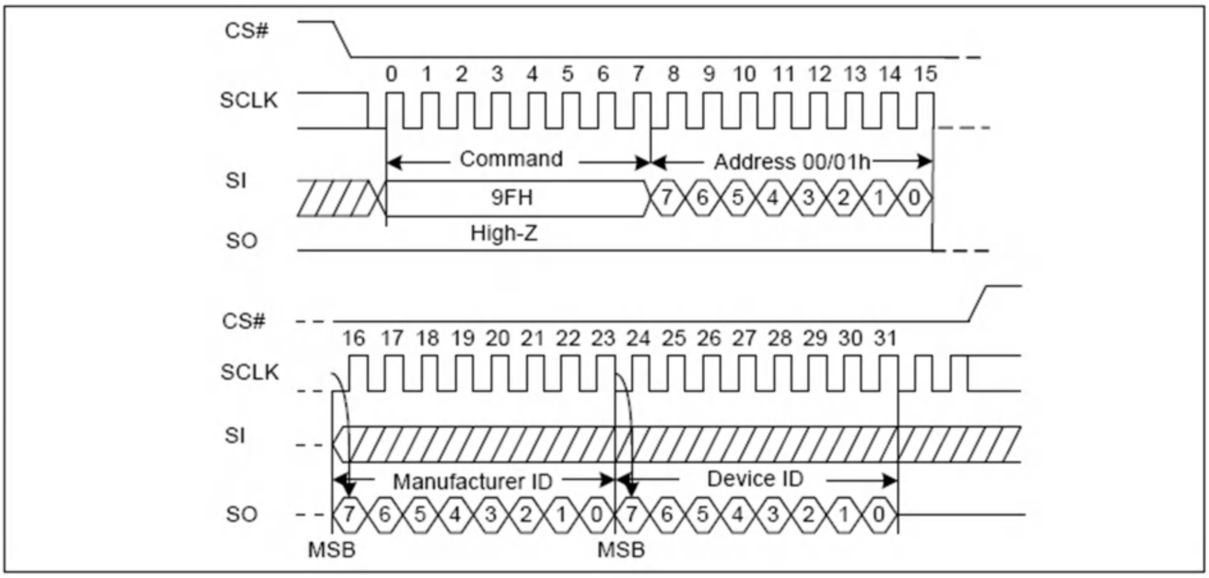


Figure 6-2 Read ID Sequence Diagram

5.3 Write Enable（WREN）（06H）

The Write Enable command (WREN) is used to enable WEL bit (set it to 1). The WEL bit must be set to 1 before using the following commands:

- Page program
- OTP program/OTP protection
- Block erase

Notes:

1. WEL bit will be automatically cleared after executing the above commands.
2. WEL bit will be automatically cleared after receiving the RESET (FFH) command.

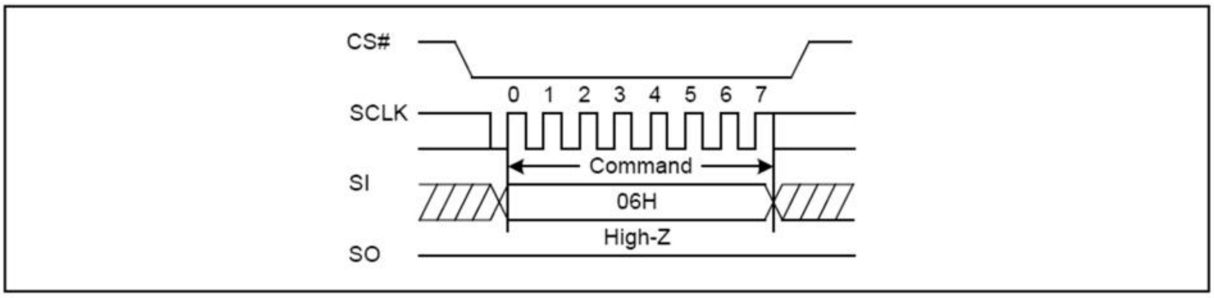


Figure 6-3 Write Enable Sequence Diagram

5.4 Write Disable（WRDI）（04H）

The Write Disable (WRDI) command is used to disable WEL (reset it to 0).

Notes: WEL will be automatically cleared after receiving the RESET (FF) command.

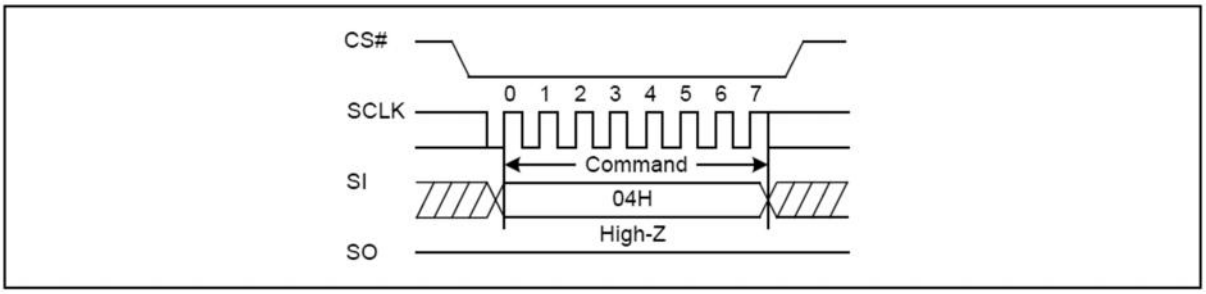


Figure 6-4 **Write Disable Sequence Diagram**

5.5 Get Features （0FH） and Set Features （1FH）

- The GET FEATURES（0FH）和 SET FEATURES（1FH）command are used to monitor and alter the working status of SPI NAND FLASH
- These commands use a 1-byte feature address to determine which feature is to be read or modified.
- The features in the feature byte B0H are all volatile except OTP_PRT bit.
- All registers have a default value after power-up (except the non-volatile bit).
- P_FAIL, E_FAIL, and WEL will be cleared after the RESET (FF) command being executed, while other registers will not be impacted.
- The value of all reserved bits is 0 (even after being set to 1).

Table 6-5 **Features Settings**

Register	**Addr.**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Protection	A0H	BRWD	reserved	BP2	BP1	BP0	INV	CMP	Reserved
Feature	B0H	OTP_PRT	OTP_EN	reserved	ECC_EN	reserved	reserved	reserved	QE
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FALL	E_FALL	WEL	OIP

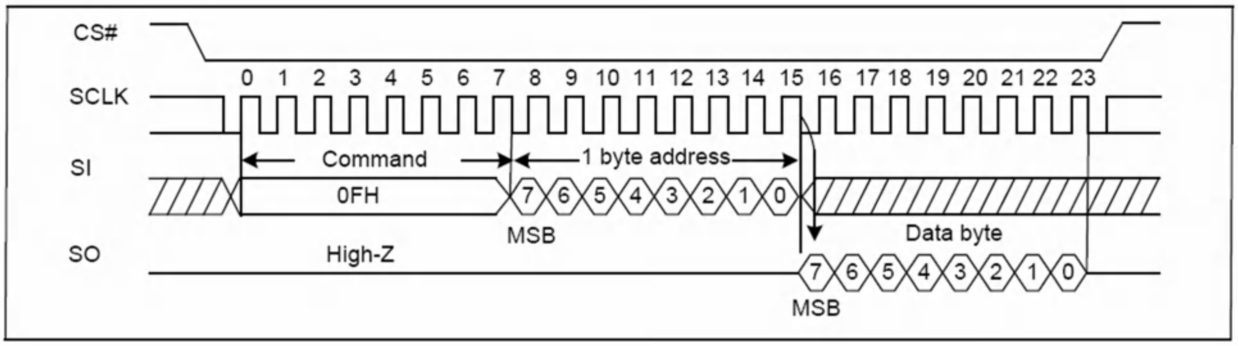


Figure 6-6 Get Features Sequence Diagram

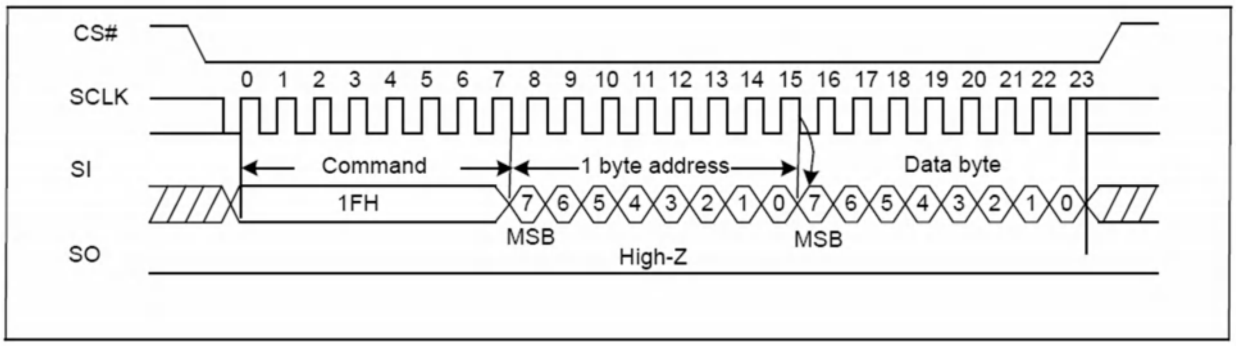


Figure 6-7 Set Features Sequence Diagram

5.6 PAGE READ OPERATIONS

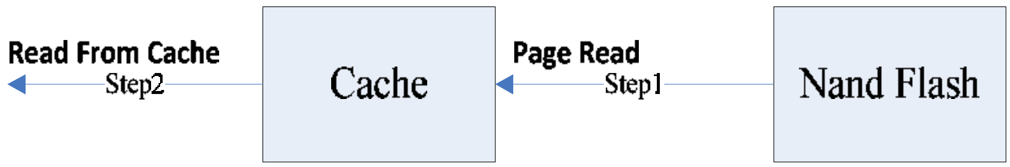


Figure 6-8 Page Read Operations Diagram

It takes three steps to read data from the SPI NAND Flash:

1. Use PAGE READ (13H) command to load the data page to the Cache.
2. Use GET FEATURES (0FH) command to check the status register (C0H). The OIP bit in status register will be HIGH until the loading operation is finished. Users may also read ECCS1 and ECCS0 to check if the data acquired is correct if ECC_EN is enabled.
3. Use READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command to read the data page from the Cache.

The address (16 bits) of the READ FROM CACHE command contains 4-bit wrap address to indicate three kinds of wrap modes and 12-bit column address to designate the starting byte address of cache. The starting byte address must be within 0 to 2111. After the end of the cache register is reached, the data wraps around the beginning boundary automatically until CS# is pulled high to terminate this operation.

Table 6-9 Wrap configure bit table

Wrap<3>	**Wrap<2>**	**Wrap<1>**	**Wrap<0>**	**Wrap Length(byte)**
0	0	X	X	2112
0	1	X	X	2048
1	0	X	X	64
1	1	X	X	16

Page Read to Cache （13H）

The PAGE READ (13H) command is used for NAND FALSH to read data and load them to the Cache (If ECC_EN is enabled, the data will be decoded in BCH before being loaded to the Cache). The address should be 24- bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 3-3 and Figure 3-4). After successfully mapping, SPI NAND FLASH will load the corresponding NAND FLASH data to the Cache. tRD represents the load time. In this process, users may use GET FEATURE (0FH) command to check the OIP (“OIP = 0” means the loading operation is finished). Then, use the READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command to read the data from the Cache.

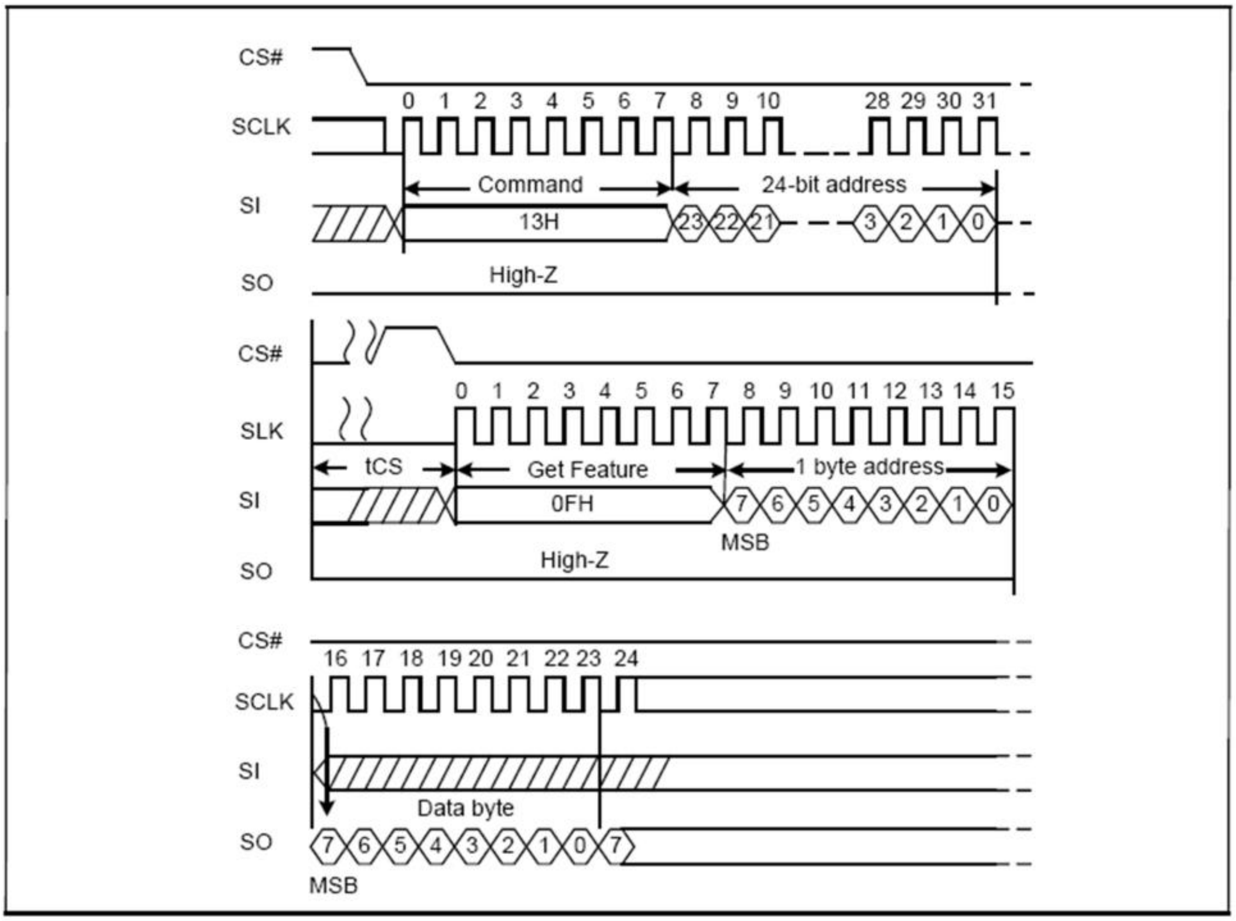


Figure 6-10 Page Read to cache Sequence Diagram

Read From Cache （03H or 0BH）

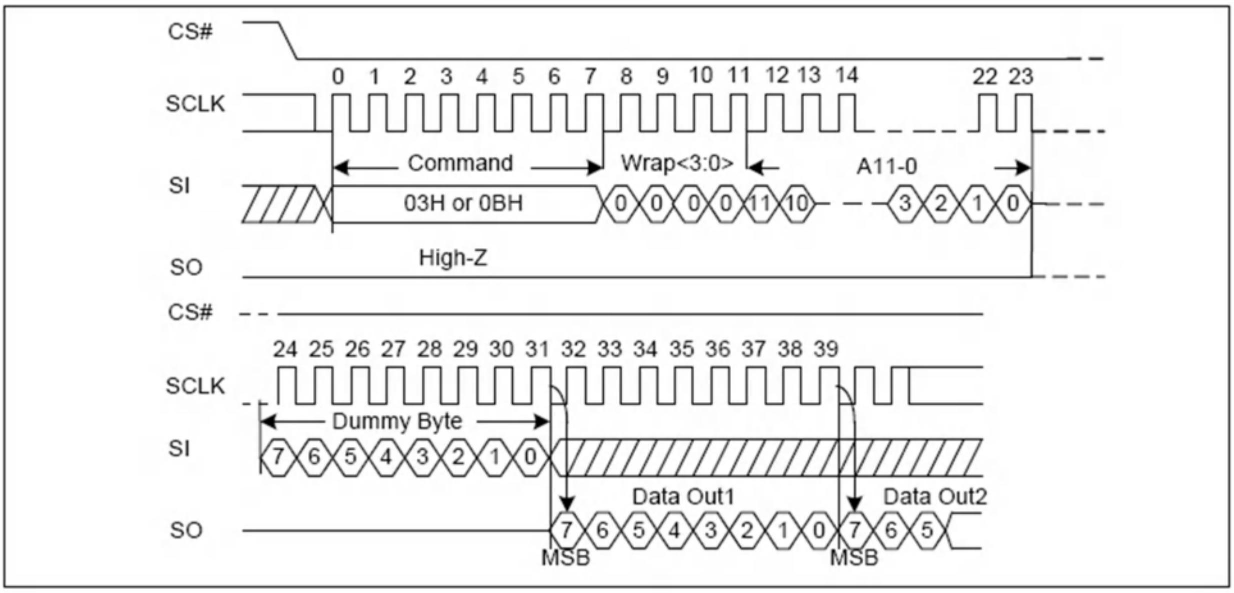


Figure 6-11 Read From Cache Sequence Diagram

Read From Cache x2 （3BH）

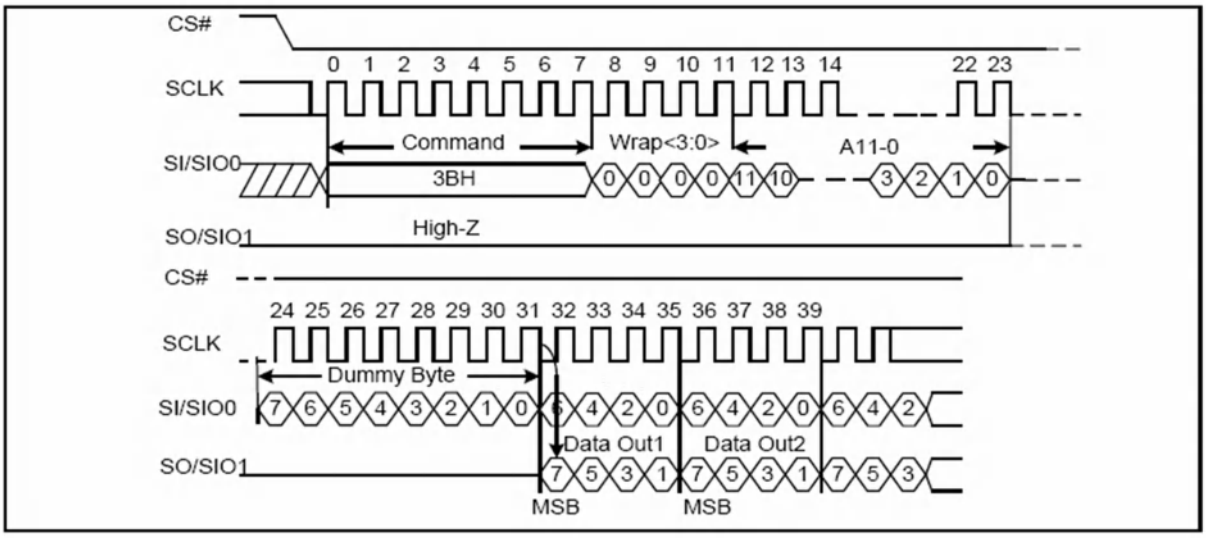


Figure 6-12 Read From Cache x2 Sequence Diagram

Read From Cache x4 （6BH）

The QE bit must be set to 1 before using the Read from Cache x4 command.

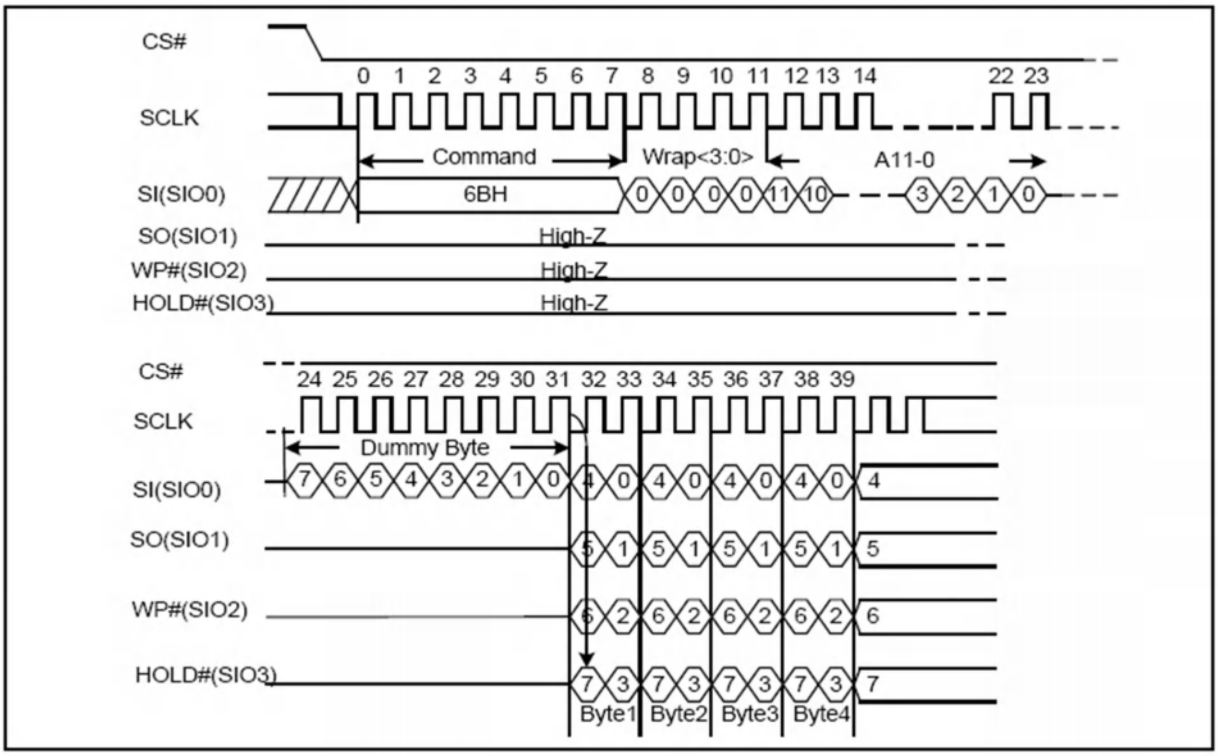


Figure 6-13 Read From Cache x4 Sequence Diagram

Read From Cache Dual IO （BBH）

The Read from Cache Dual I/O demand (BBH) is similar to Read from Cache x2 command (3BH), but the address fields (wrap<3:0> A11-0) are transmitted by SIO0 and SIO1.

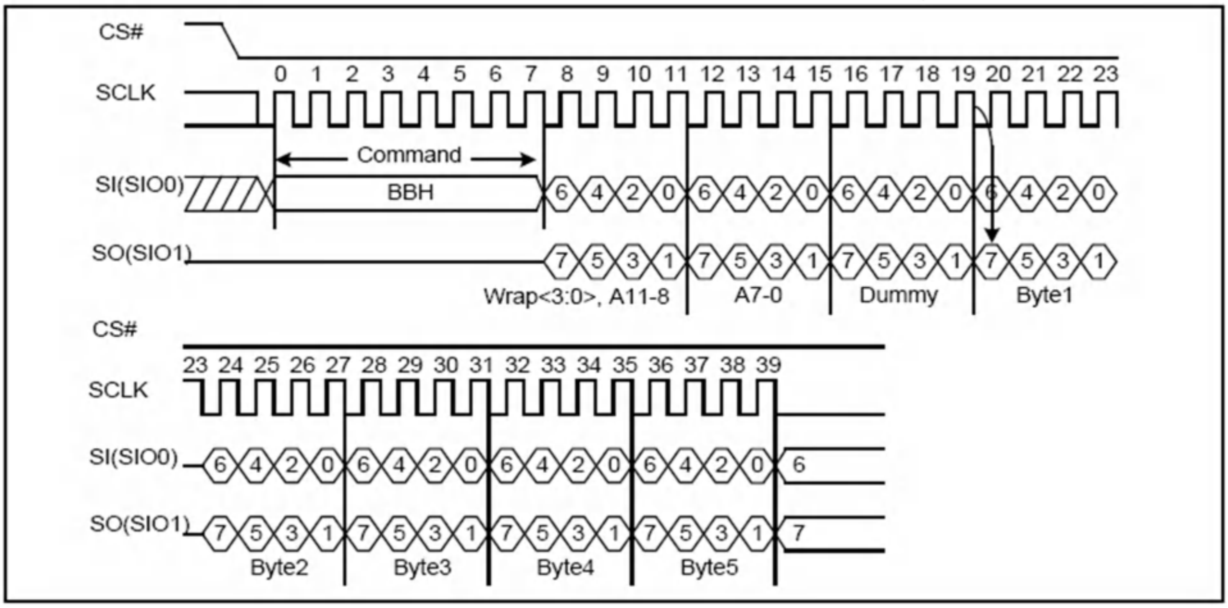


Figure 6-14 Read From Cache Dual IO Sequence Diagram

Read From Cache Quad IO （EBH）

The Read from Cache Quad IO Dual I/O command (EBH) is similar to Read from Cache x4 command (6BH), but the —18— address fields (wrap<3:0> A11-0) are transmitted by SIO0, SIO1, SIO2 and SIO3. Before using this command, the QE bit must be set to 1.

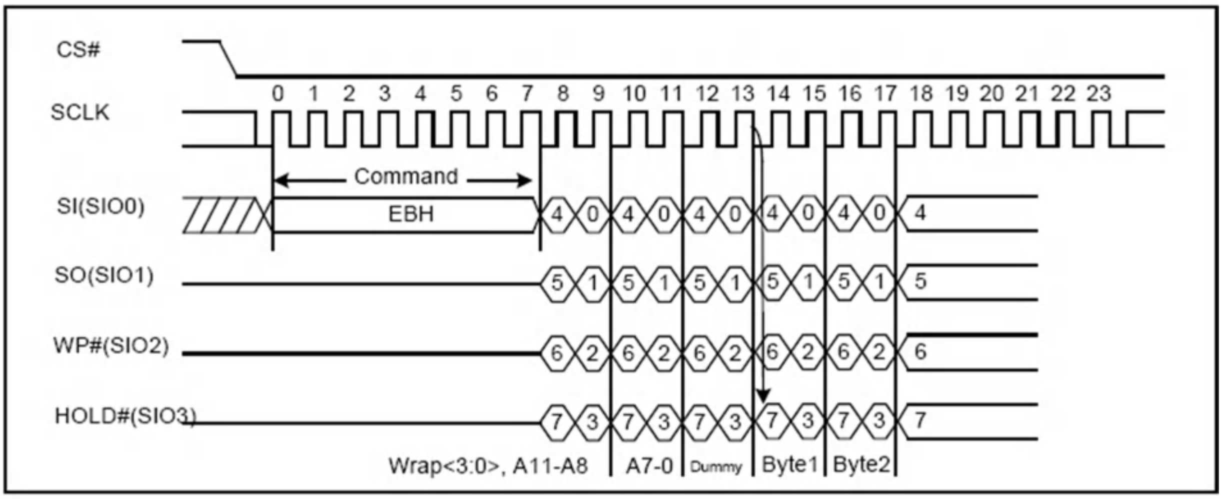


Figure 6-15 Read From Cache Quad IO Sequence Diagram

5.7 PAGE PROGRAM OPERATIONS

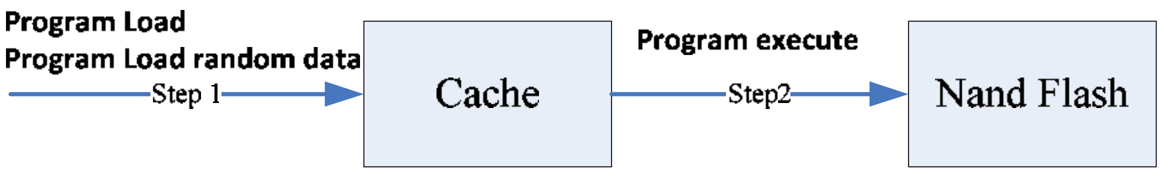


图 6-16 Page Program Operations Diagram

It takes four steps to write data to the SPI NAND Flash:

1. Use the PROGRAM LOAD (02H/32H) command or PROGRAM LOAD RANDOM DATA (84H/C4H/ 34H/72H) command to load the data page to the Cache;

2. WRITE ENABLE (06H);

3. Use the PROGRAM EXECUTE (10H) command to program the data page into the NAND FLASH.

4. Use the GET FEATURES (0FH) command to check the status register (C0H) until the program operation is accomplished (OIP = 0). Check P_FAIL to make sure if the program operation is successful or not ("P_FAIL= 0" means success).

According to different program requirements, the specific commands sequence used are as follows:

➢ Program Load &Page Program

The PROGRAM LOAD is used to program 1-to-2112-byte data into the NAND FLASH and the commands sequence are as follows:

- 02H （PROGRAM LOAD）/32H （PROGRAM LOAD x4）
- 06H （WRITE ENABLE）
- 10H （PROGRAM EXECUTE）
- 0FH （GET FEATURE）

The address of the PROGRAM LOAD (02H/32H) command contains 4 dummy bits and 12-bit column address. It is used to load data into the Cache. If more than 2112 bytes are loaded, the additional bytes will be ignored. Issue the WRITE ENABLE (06H) command to set WEL to 1. If WEL = 0, the subsequent program operation will be ignored and P_FAIL=0. Then use the PROGRAM EXECUTE (10H) command to write the data in the Cache into the NAND FLASH. Use GET FEATURE (0FH) command to check the program result. "OIP = 0" means the program operation is completed, and "P_FAIL= 0" means the operation is successful. If P_FAIL=1, the program operation fails and the user can refer to the description of P_FAIL in the status register for detailed causes.

➢ Internal Data Move &Page Program

PROGRAM LOAD RANDOM DATA is used to alter portion or all of the data in the cache. Similar to the "Copy back" operation in NAND FLASH, the command sequence used are as follows:

- 13H （PAGE READ to cache）
- 84H/C4H/ 34H（PROGRAM LOAD RANDOM DATA）
- 84H/C4H/ 34H（PROGRAM LOAD RANDOM DATA）
- ……

- 06H （WRITE ENABLE）
- 10H （PROGRAM EXECUTE）
- 0FH （GET FEATURE）

Issue a PAGE READ (13H) command to read out the NAND FLASH page data that need altering into the cache and then issue a PROGRAM LOAD RANDOM DATA (84H/C4H/72H) command to update bytes of data in the page. Use WRITE ENABLE (06H) demand to set WEL to 1 and enable write. If WEL = 0, the subsequent programming will be ignored. Then issue a PROGRAM EXECUTE (10H) command to program the data in the Cache into the NAND FLASH. Use a GET FEATURE (0FH) command to check the program result. “OIP = 0” means the program operation is completed, and “P_FAIL= 0” means the program is successful. If P_FAIL=1, the program fails and users can refer to the description of P_FAIL in the status register for detailed causes.

Program Execute (PE) (10H)

PROGRAM EXECUTE (10H) is used to program the data from the cache into the NAND FLASH. The address should be 24-bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 3-3 and Figure 3-4). After successfully mapping, the data in the cache begin to program. tRD means the transferring time. In this process, users may use the GET FEATURE (0FH) command to check the OIP (“OIP = 0” means the operation is finished).

Data should be loaded into the cache before using the PROGRAM EXECUTE (10H) command, and there are two ways to load cache data: Program Load and Program Load Random Data.

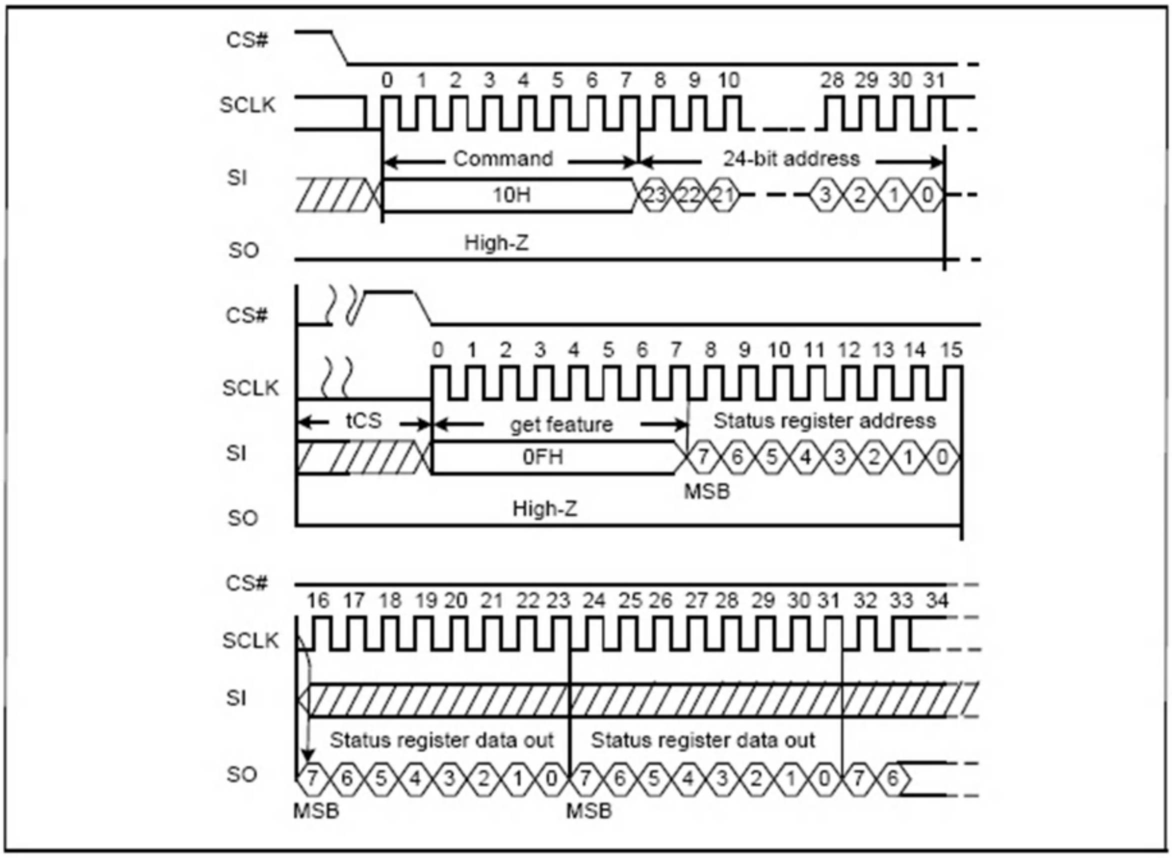


Figure 6-17 Program Execute Sequence Diagram

Program Load （PL） （02H）

The PROGRAM LOAD (02H) command address contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the data transfer process or the transfer process will be forced to terminate.

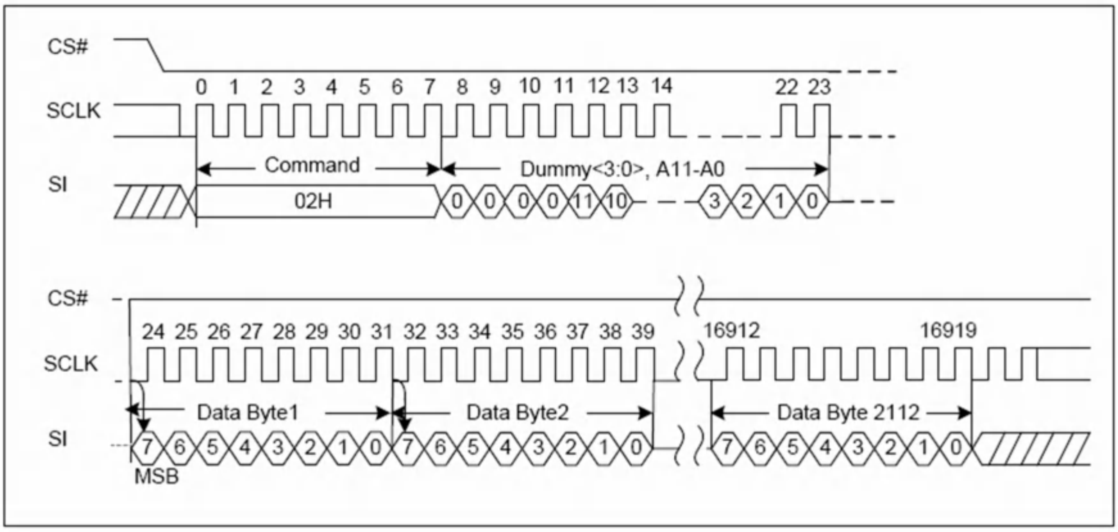


Figure 6-18 Program Load Sequence Diagram

Program Load x4 （PL x4） （32H）

The PROGRAM LOAD x4 (32H) command address contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. The QE bit must be set to 1 before using the Program Load x4 command. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate.

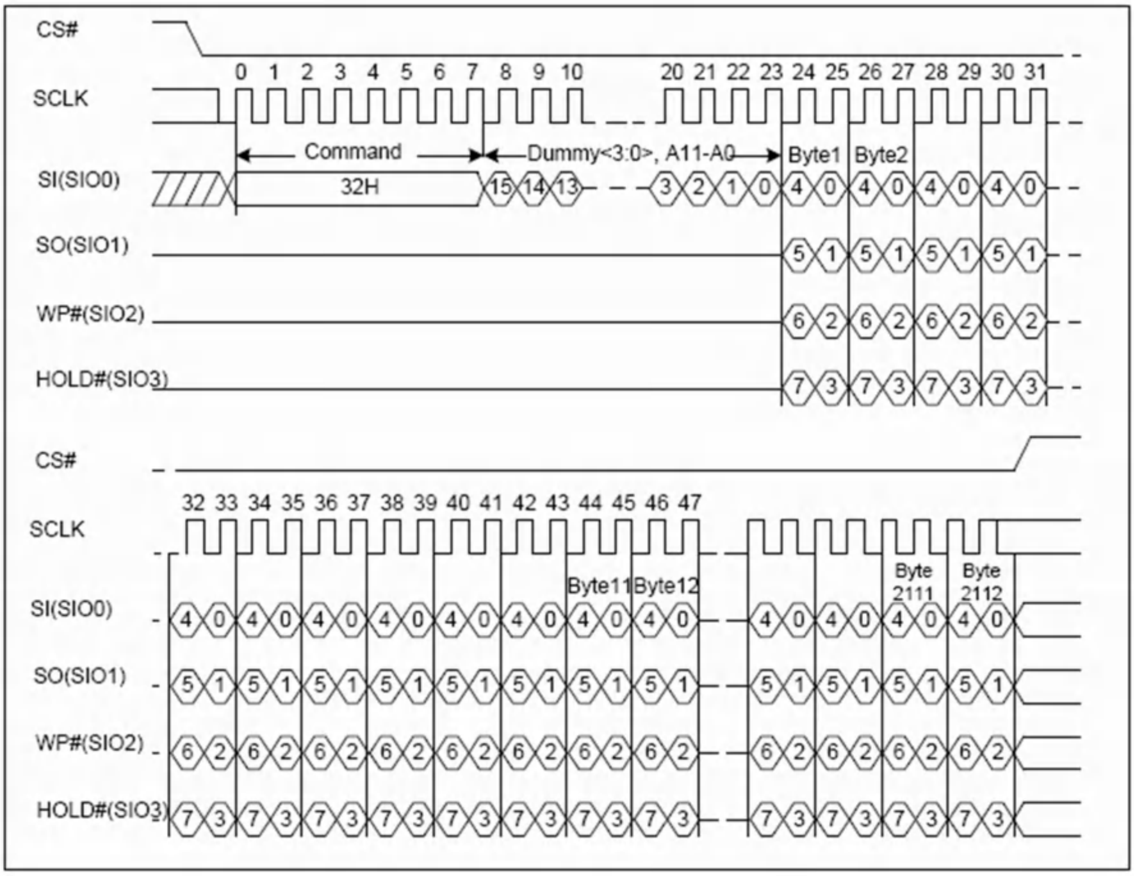


Figure 6-19 Program Load x4 Sequence Diagram

Program Load Random Data （84H）

The PROGRAM LOAD RANDOM DATA (84H) command contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate.

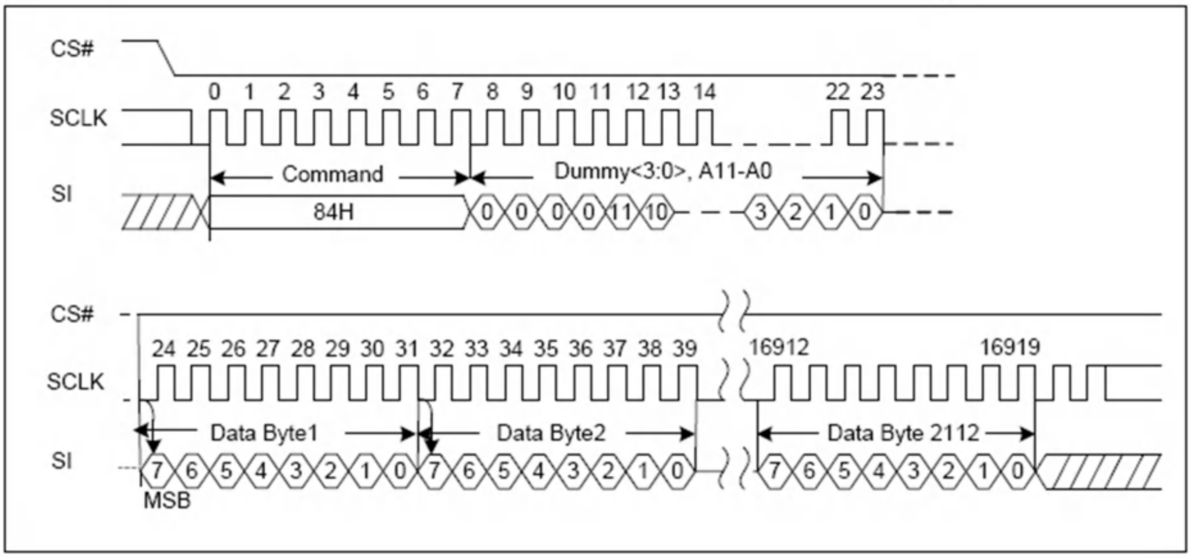


Figure 6-20 Program Load Random Data Sequence Diagram

Program Load Random Data x4 （C4H/34H）

The PROGRAM LOAD RANDOM DATA x4 (C4H/34H) command contains 4 dummy bits and 12-bit column address. The 12-bit column address is used to locate the starting byte address. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate. The QE bit must be set to 1 before using the command.

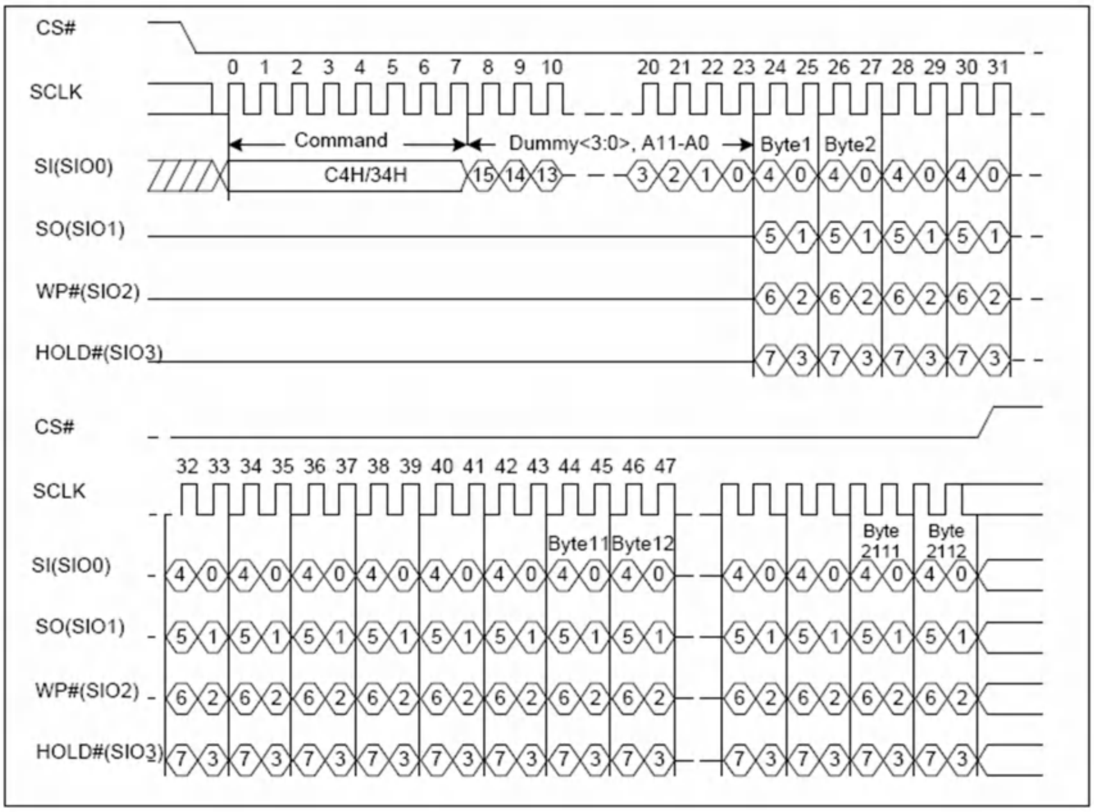


Figure 6-21 Program Load Random Data x4 Sequence Diagram

Program Load Random Data Quad IO （72H）

The Program Load Random Data Quad IO (EBH) command is similar to the PROGRAM LOAD RANDOM DATA x4(C4H/34H) command, but the address fields (dummy<3:0> A11-0) are transmitted by SIO0, SIO1, SIO2, and SIO3. The QE must be set to 1 before using the command. If more than 2112 bytes are loaded, the additional bytes will be ignored. The CS# should not be set to high during the transfer process or the transfer process will be forced to terminate。

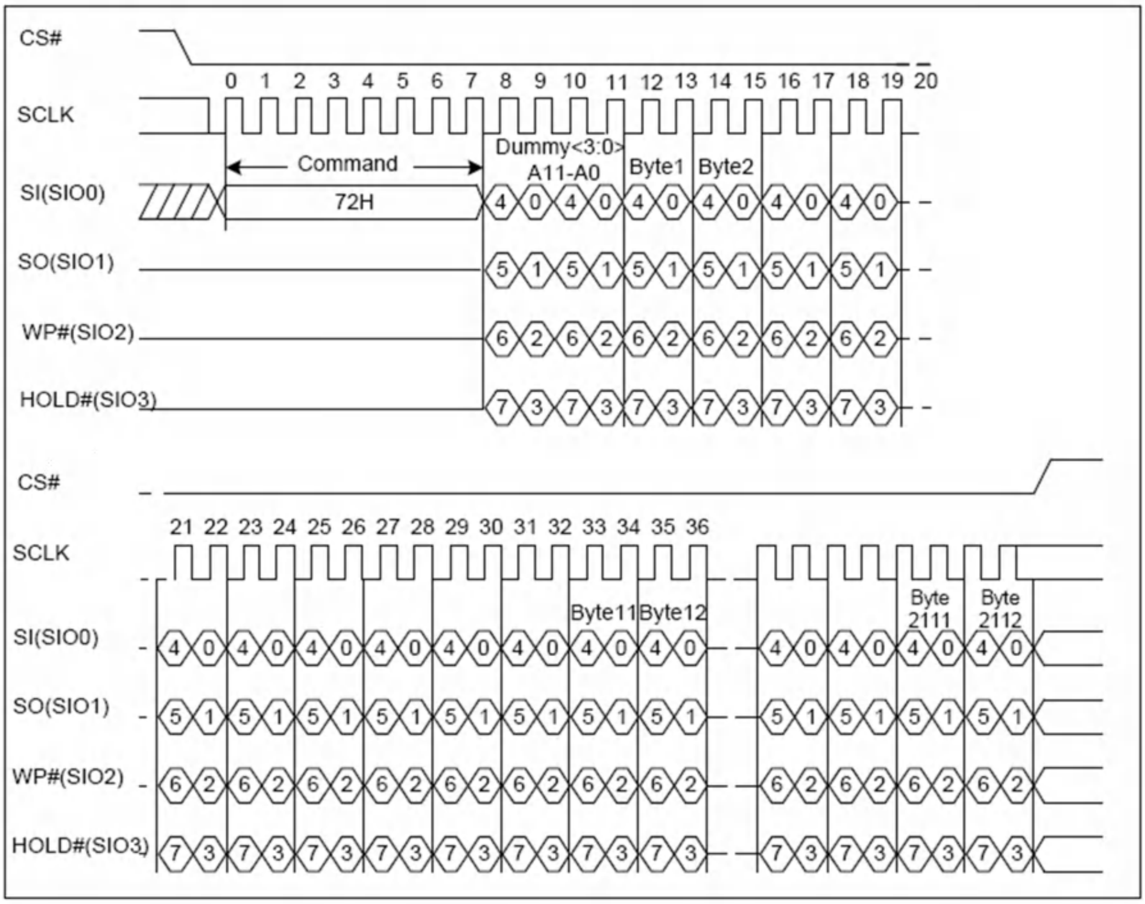


Figure 6-22 Program Load Random Data Quad IO Sequence Diagram

5.8 ERASE OPERATIONS Block Erase （D8H）

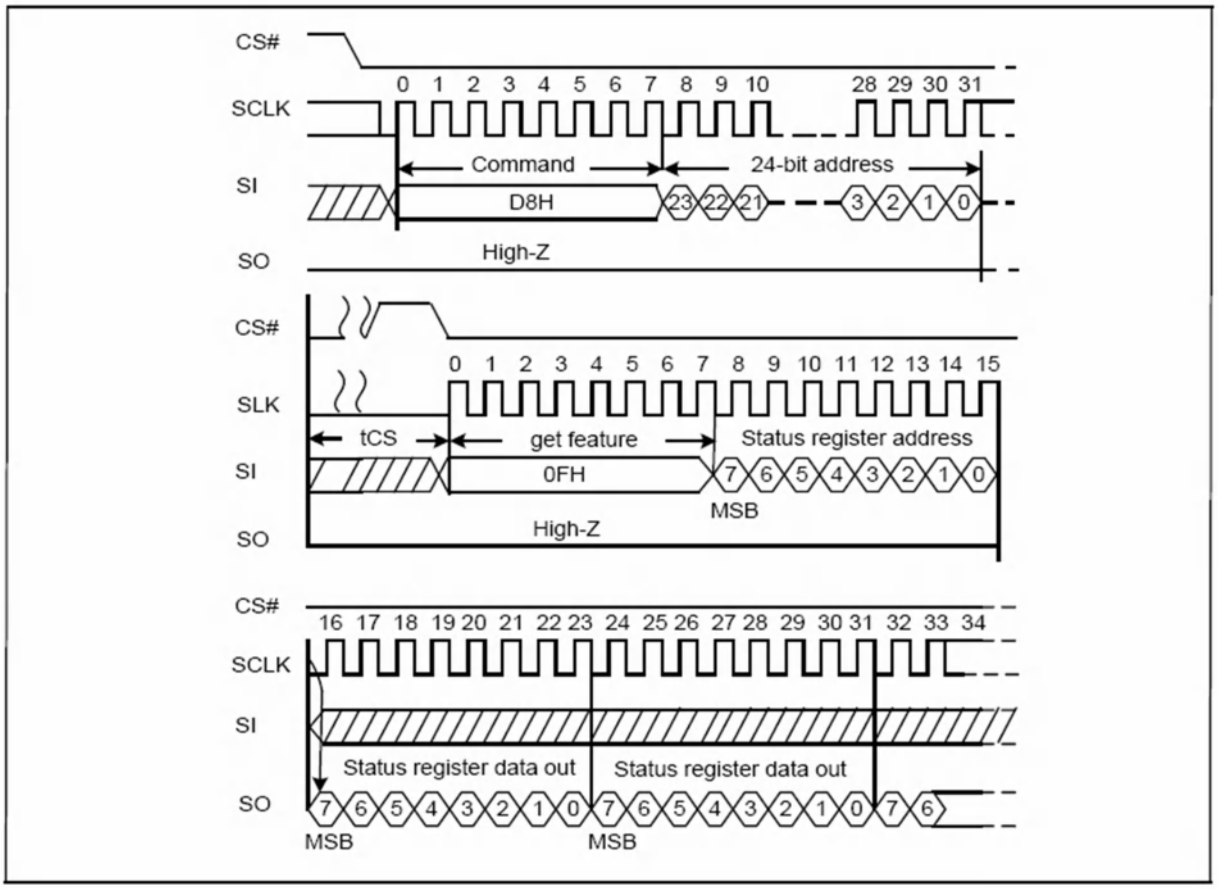


Figure 6-23 Block Erase Sequence Diagram

The BLOCK ERASE (D8H) command is used to erase the NAND FLASH block. The address of this command is 24-bit, and the length of the Page / Block address depends on the specifications of the Flash (refer to Figure 3-3 and Figure 3-4). After successfully mapping, the erase operation begins. tERS means the busy time of erase process. In this process, users may issue a GET FEATURE (0FH) command to check the OIP and monitor the erase results. “OIP = 0” means the erase operation is finished, and “E_FAIL= 0” means the operation is successful. If E_FAIL = 1, the operation fails and users can refer to the description of P_FAIL in the status register for detailed causes.。

While a BLOCK ERASE (D8H) command is in progress (OIP = 1), users can use a READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH) to read the cache or use a PROGRAM LOAD command (02H/32H/84H/C4H/ 34H/72H) to write the cache.

The commands sequence is as follows:

- 06H （WRITE ENABLE）
- D8H（BLOCK ERASE）
- 0FH （GET FEATURE）

6 SPI NAND Functional Features

6.1 OTP Region

SPI NAND FLASH provides a special One-Time Programmable memory area. The OTP region size is four pages and each page is 2112-byte. Users can use this region any way they want, like programming serial numbers or storing backup data tables.

Table 7-1 Feature Register

Register	Addr.	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Feature	B0H	OTP_PRT	OTP_EN	Reserved	ECC_EN	Reserved	Reserved	Reserved	QE
-	-	Non-volatile	Read& Write	-	Read& Write	-	-	-	Read& Write

When delivered from factory, the OTP_PRT bit is 0.To use the OTP, users should issue a SET FEATURES command to set the OTP_EN bit of the Feature Register. The PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) and PROGRAM EXECUTE (10H) commands can be used to program Page 00 to 03. Also, the PAGE READ (13H) and READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) commands can be used to read the OTP area. To lock the OTP region, users should first use the SET FEATURES command to set the OTP_EN bit and the OTP_PRT bit of the Feature Register and then use the PROGRAM EXECUTE (10H) command to finish locking.

Table 7-2 OTP States

OTP_PRT	OTP_EN	State
X	0	Normal operation; access the user's host storage.
0	1	Access the OTP region (read and program) Notes: "**OTP_PRT = 0**" means that the OTP is not locked yet. The OTP can be programmed many times, but the OTP pages that have been programmed cannot be programmed again, otherwise there will cause unexpected results.
1	1	1. When **OTP_PRT is 0**, users can set OTP_PRT and OTP_EN to 1 and then issue a PROGRAM_EXECUTE (10H) command to lock the OTP. After that, the OTP_PRT will permanently remain 1 (no matter the device is powered up or not). 2. When the **OTP_PRT is 1**, users can only read the OTP region.

Enter the OTP Mode

- Issue a SET FEATURES (1FH) command
- Feature register B0H
- Set the OTP_EN bit to 1

Access the OTP Date

- Issue a PAGE READ (13H) command after entering the OTP mode.

- Issue a READ FROM CACHE command (03H/0BH/3BH/6BH/BBH/EBH) to read out data from the cache.

Write Data into OTP (only when OTP_PRT is 0)

- Enter the OTP mode
- Issue the WRITE ENABLE (06H) command
- Use the PROGRAM LOAD (02H/32H) or PROGRAM RANDOM (84H/C4H/34H/72H) command to write data into the cache
- Issue the PROGRAM EXECUTE (10H) command
- Use the GET FEATURES (OFH) command to check if the operation is finished (“OIP = 0” means it is finished, and “P_FAIL = 0” means it is successful)
- Repeat step 2 and its subsequent steps and use the OTP address to program

Lock the OTP Region

- Use SET FEATURES (1FH) command to set the OTP_EN and OTP_PRT bit
- Issue the WRITE ENABLE (06H) command
- Issue the PROGRAM EXECUTE (10H) command

  After the OTP region is locked, the OTP_PRT bit will be forever 1 and the OTP region cannot be erased or programmed again.

6.2 Status Register

The SPI NAND FLASH has an 8-bit status register that software can read during the device operation for operation state query, such as the ECC results of read operations (ECCS1 and ECCS0), the program results (P_FAIL), and the end of operations (OIP).

This register can be read by issuing the GET FEATURES (OFH) command followed by the feature address (C0H).

Table 7-3 Status Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Status	C0H	Reserved	Reserved	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
—	—	—	—	Read only	Read only	Read only	Read only	Read only	Read only

Table 7-4 Description of Status Register

Bit-field	Bit name	Description
P_FAIL	Program results	P_FAIL = 0： Program OK P_FAIL = 1： Program FAIL **Notes: Possible causes for P_FAIL to be 1:** The user programs an invalid address; The user programs a locked and protected OTP region; The users programs a protected region (BP0, BP1, BP2，INV, CMP). **Notes: Causes for reset:**

Bit-field	Bit name	Description
		The bit is cleared during the PROGRAM EXECUTE command sequence; The bit is cleared after receiving a reset command (FFH). 编程被保护的区域（BP0, BP1, BP2，INV, CMP）
E_FAIL	Erase results	E_FAIL = 0: erase OK E_FAIL = 1: erase fail **Notes: Possible causes for E_FAIL to be 1:** The user erases an invalid address; The user erases an OTP region; The user erases a protected region (BP0, BP1, BP2，INV, CMP). **Notes: Causes for reset:** The bit is cleared at the start of the BLOCK ERASE command sequence; The bit is cleared after receiving a RESET(FFH) command.
WEL	Enable write	This bit indicates the current status of the WRITE_ENABLE (WEL = 1), WRITE_DISABLE, and (WEL = 0) commands. WEL must be 1 before using the PROGRAM_EXECUTE (10H) and the BLOCK_RASE (D8H) commands. Otherwise, the execution of the commands is invalid.
OIP	Operation in progress	OIP indicates if the PAGE_READ (13H), PROGRAM_EXECUTE (10H) and BLOCK_RASE (D8H) commands are in progress. When using the RESET (FFH) command after powering up, OIP indicates the current status of the internal initialization. When using the RESET (FFH) command during operation, OIP indicates the current status of the stopping operation. Notes: “OIP = 0” means the operation is accomplished and “OIP = 1” means the operation is in progress.
ECCS1,ECSS0	BCH status	00: no error was detected during the execution of PAGE_READ (13H) command. 01: errors were detected and corrected. 10: Uncorrectable errors were detected. 11: 8 bits errors were detected and corrected. Errors over 8 bits cannot be corrected. **Notes: Causes for reset:** The bit is cleared at the beginning of the PAGE_READ (13H) command. The bit indicates the loading results of Block 0 and Page 0 after powering up and reset. (The reset command (FFH) and powering up will automatically loads Block 0 and Page 0 to the cache.)

6.3 Internal ECC

SPI NAND FLASH provides data protection by offering internal ECC. The ECC can be enabled by setting feature bit ECC_EN. The default ECC_EN is enabled (ECC_EN = 1) after power-up and reset. Users can perform the following command sequence to enable or disable the ECC_EN.

- Issue the SET FEATURES (1FH) command;
- Set ECC_EN to 1 to enable ECC; set ECC_EN to 0 to disable ECC.

After the ECC is enabled and during a PROGRAM operation, the device calculates an ECC code on the 2K data in the cache and then write them into the NAND FLASH. During a READ operation, the device decodes the 2K data read out from the NAND FLASH with ECC, then write them in the cache, and show the decoding results in the ECCS1 and ECCS0. For the pages that have been erased but not programmed, the ECCS1 and ECCS0 will always be 0 during a READ operation no matter ECC_EN is 0 or 1. For the Flash with Page size 2176 bytes, See Table 7-5 for more details.

Table 7-5 **ECC Protection and Spare Area（2176 bytes per page）**

Starting Byte Address	Ending Byte Address	ECC Protection	Area	Size	Description
000H	1FFH	Yes	Main0	512	User data 0
200H	3FFH	Yes	Main1	512	User data 1
400H	5FFH	Yes	Main2	512	User data 2
600H	7FFH	Yes	Main3	512	User data 3
800H	803H	Yes	Spare0	3	User Meta 0 I
804H	80BH	Yes	Spare0	9	User Meta 0 II
80CH	80FH	Yes		4	ECC for Meta 0 II
810H	813H	Yes	Spare1	3	User Meta 1 I
814H	81BH	Yes	Spare1	9	User Meta 1 II
81CH	81FH	Yes		4	ECC for Meta 1 II
820H	823H	Yes	Spare2	3	User Meta 2 I
824H	82BH	Yes	Spare2	9	User Meta 2 II
82CH	82FH	Yes		4	ECC for Meta 2 II
830H	833H	Yes	Spare3	3	User Meta 3 I
834H	83BH	Yes	Spare3	9	User Meta 3 II
83CH	83FH	Yes		4	ECC for Meta 3 II
840H	87FH	Yes	Internal ECC	64	ECC for main(0~3) and Meta(0~3) I

Notes:

1. When ECC is enabled, data write operation into the ECC area will be ignored.

ECC Protection and Spare Area（2112 bytes per page）	Ending Byte Address	ECC Protection	Area	Size	Description
000H	1FFH	Yes	Main0	512	User data 0

ECC Protection and Spare Area（2112 bytes per page）	Ending Byte Address	ECC Protection	Area	Size	Description
200H	3FFH	Yes	Main1	512	User data 1
400H	5FFH	Yes	Main2	512	User data 2
600H	7FFH	Yes	Main3	512	User data 3
800H	803H	Yes	Spare0	3	User Meta 0
804H	80FH	Yes		13	ECC for Main0 and Spare0
810H	813H	Yes	Spare1	3	User Meta 1
814H	81FH	Yes		13	ECC for Main1 and Spare1
820H	823H	Yes	Spare2	3	User Meta 2
824H	82FH	Yes		13	ECC for Main2 and Spare2
830H	833H	Yes	Spare3	3	User Meta 3
83CH	83FH	Yes		13	ECC for Main3 and Spare3

6.4 Block Protection

Table 7-9 Protection Register

Register	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Protection	A0H	BRWD	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
—	—	Read & Write	—	Read & Write	Read & Write	Read & Write	Read & Write	Read & Write	Read & Write

- Issue GET FEATURES (0FH) and SET FEATURES (1FH) commands to read or set the Protection Register.
- SPI NAND provides write protection for all device or portion of the blocks, and all blocks are under the default write protection after power-up (BP2, BP1, BP0 = 1).
- When BRWD is 1 and WP# is low, all protected bits cannot be altered by the SET FEATURES (1FH) command.
- PROGRAM/ERASE command being issued to a locked block will lead to operation error (P_FAIL= 1/EFAIL= 1).
- See Table 6-10 for the protected page address of the write protection bits (BP0, BP1, BP2，INV, CMP) of different capacity (take the 64-page-per-block Flash as an example).

Table 7-10 Block Lock Register Block Protect Bits(64 pages per block)

CMP	INV	BP2	BP1	BP0	Protect page Address （1024 Blocks）	Protect page Address （2048 Blocks）	Protect page Address （4096 Blocks）	Protect Rows
X	X	0	0	0	None	None	None	UNLOCK
X	X	1	1	1	0000H-FFFFH	00000H-1FFFFH	0000H-3FFFFH	LOCK
0	0	0	0	1	FC00H-FFFFH	1F800H-1FFFFH	3F000H-3FFFFH	H 1/64
0	0	0	1	0	F800H-FFFFH	1F000H-1FFFFH	3E000H-3FFFFH	H 1/32
0	0	0	1	1	F000H-FFFFH	1E000H-1FFFFH	3C000H-3FFFFH	H 1/16
0	0	1	0	0	E000H-FFFFH	1C000H-1FFFFH	38000H-3FFFFH	H 1/8
0	0	1	0	1	C000H-FFFFH	18000H-1FFFFH	30000H-3FFFFH	H 1/4
0	0	1	1	0	8000H-FFFFH	10000H-1FFFFH	20000H-3FFFFH	H 1/2
0	1	0	0	1	0000H-03FFH	0000H-07FFH	0000H-0FFFH	L 1/64
0	1	0	1	0	0000H-07FFH	0000H-0FFFH	0000H-1FFFH	L 1/32
0	1	0	1	1	0000H-0FFFH	0000H-1FFFH	0000H-3FFFH	L 1/16
0	1	1	0	0	0000H-1FFFH	0000H-3FFFH	0000H-7FFFH	L 1/8
0	1	1	0	1	0000H-3FFFH	0000H-7FFFH	0000H-FFFFH	L 1/4
0	1	1	1	0	0000H-7FFFH	0000H-FFFFH	0000H-1FFFFH	L 1/2
1	0	0	0	1	0000H-FBFFH	0000H-1F7FFH	0000H-3FFFH	L 63/64
1	0	0	1	0	0000H-F7FFH	0000H-1EFFFH	0000H-3DFFFH	L 31/32
1	0	0	1	1	0000H-EFFFH	0000H-1DFFFH	0000H-3BFFFH	L 15/16
1	0	1	0	0	0000H-DFFFH	0000H-1BFFFH	0000H-37FFFH	L 7/8
1	0	1	0	1	0000H-BFFFH	0000H-17FFFH	0000H-2FFFFH	L 3/4
1	0	1	1	0	0000H~003FH	0000H~003FH	0000H~0003FH	Block0
0	1	0	0	1	0400H-FFFFH	0800H-1FFFFH	1000H-3FFFFH	H 63/64
0	1	0	1	0	0800H-FFFFH	1000H-1FFFFH	2000H-3FFFFH	H 31/32
0	1	0	1	1	1000H-FFFFH	2000H-1FFFFH	4000H-3FFFFH	H 15/16
0	1	1	0	0	2000H-FFFFH	4000H-1FFFFH	8000H-3FFFFH	H 7/8
0	1	1	0	1	4000H-FFFFH	8000H-1FFFFH	10000H-3FFFFH	H 3/4
0	1	1	1	0	0000H~003FH	0000H~003FH	00000H~0003FH	Block0

6.5 Block 0 Page 0 Automatically Loads to Cache

SPI NAND will automatically load the data in Block 0 Page 0 with ECC decode during power-up process. Data can be read out of the cache by using the READ FROM CACHE (03H/0BH/3BH/6BH/BBH/EBH) command.

When the SPI NAND wake up from sleep mode it will also load the data in Block 0 Page 0 to the cache with ECC decode.

7 POWER ON TIMING

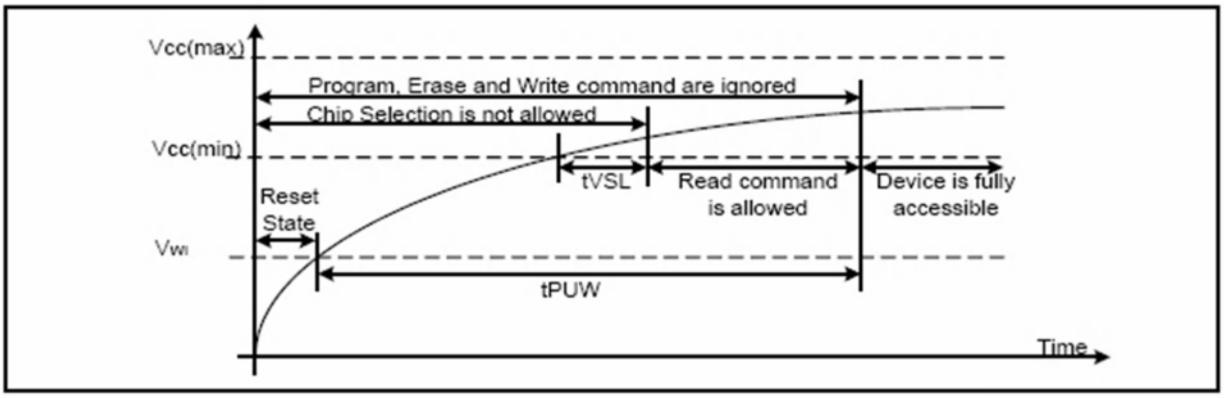


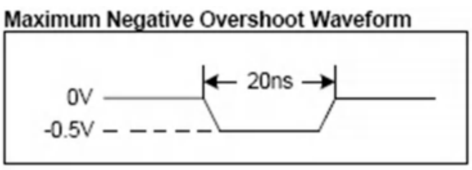
Figure 7-1 Power on Timing Sequence

Table 7-1 Power-On Timing and Write Inhibit Threshold for 3.3V

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To CS# LOW		1	ms
tPUW	Time Delay From $VCC_{(WI)}$ To Write Instruction		1.5	ms
VWI	Write Inhibit Voltage		2.9	V

Table 7-2 ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85	℃
Storage Temperature	-55 to 125	℃
Applied Input/Output Voltage	-0.5 to 4.0	V
VCC	-0.5 to 4.0	V



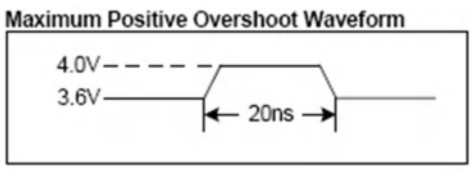


表 7-3 CAPACITANCE MEASUREMENT CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
CIN	Input Capacitance			6	pF	
COUT	Output Capacitance			10	pF	
C_L	Load Capacitance			30	pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.2*VCC		0.8*VCC	V	
	Input Timing Reference Voltage	0.3*VCC		0.7*VCC	V	
	Output Timing Reference Voltage		0.5*VCC		V	

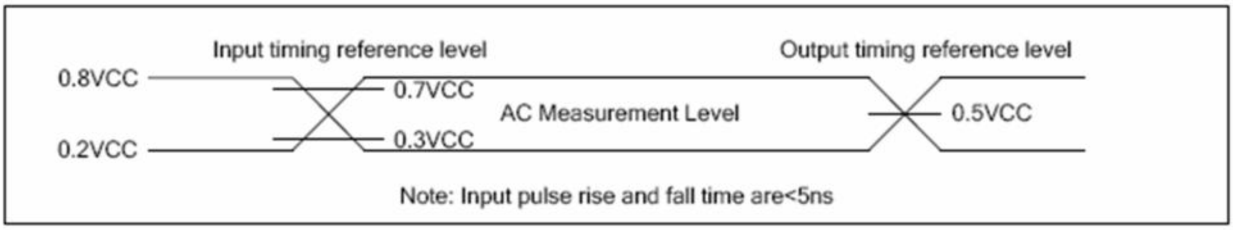


Figure 7-2 Input Test Waveform And Measurement Level

8 Electrical Characteristics

8.1 DC Characteristics

Table 8-1 DC Characteristic

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current				±2	uA
I_{LO}	Output Leakage Current				±2	uA
I_{CC1}	Standby Current	CS# = VCC V_{IN} = VCC or VSS			90①/108 ②/126③	uA
I_{CC2}	Operation Current(Read)	CLK = 0.1VCC/0.9VCC At 104MHz，Q = Open(*1 I/O)				mA
		CLK = 0.1VCC/0.9VCC At 80MHz，Q=Open(*1,*2,*4 I/O)			35	mA
V_{IL}	Input Low Voltage		-0.5		0.3VCC	V
V_{IH}	Input High Voltage		0.7VCC		VCC+0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA			0.3	V
V_{OH}	Output High Voltage	I_{OH} = 100uA	VCC-0.1			V

(T= -40℃~85℃, VCC=2.7~3.6V)

① 1.8V flash,16bit

② 3.3V flash 16bit

③ 3.3V flash 8bit

8.2 AC Characteristics

Table 8-2 AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_C	Serial Clock Frequency For: all command			90	MHz
t_{CH}	Serial Clock High Time	5.5			ns
t_{CL}	Serial Clock Low Time	5.5			ns
t_{CLCH}	Serial Clock Rise Time(Slew Rate)	0.5			V/ns
t_{CHCL}	Serial Clock Fall Time(Slew Rate)	0.5			V/ns
t_{SLCH}	CS# Active Setup Time	5			ns
t_{CHSH}	CS# Active Hold Time	5			ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	1			ns

Symbol	Parameter	Min	Typ	Max	Unit
t_{DVCH}	Data in Setup Time	3			ns
t_{CHDX}	Data in Hold Time	5			ns
t_{HLCH}	Hold# Low Setup Time(relative to Clock)	5			ns
t_{HHCH}	Hold# High Setup Time(relative to Clock)	5			ns
t_{CHHL}	Hold# Low Hold Time(relative to Clock)	5.5			ns
t_{CHHH}	Hold# High Hold Time(relative to Clock)	5.5			ns
t_{HLQZ}	Hold# Low to High-Z Output			10	ns
t_{HHQX}	Hold# High to Low-Z Output			10	ns
t_{CLQV}	Clock Low to Output Valid			9	ns
t_{WHSL}	WP# Setup Time Before CS# Low	20			ns
t_{SHWL}	WP# Hold Time After CS# High	100			ns

(T= -40℃~85℃, VCC=2.7~3.6V, C_L=30pf)

8.3 PERFORMANCE TIMING

Table 8-3 PERFORMANCE TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t_{RST}	CS# High To Next Command After Reset(FFh)			500	us
t_{RD}	Read From Array			120	us
t_{PROG}	Page Program Time		0.5	1	ms
t_{BERS}	Block Erase Time		3	5	ms

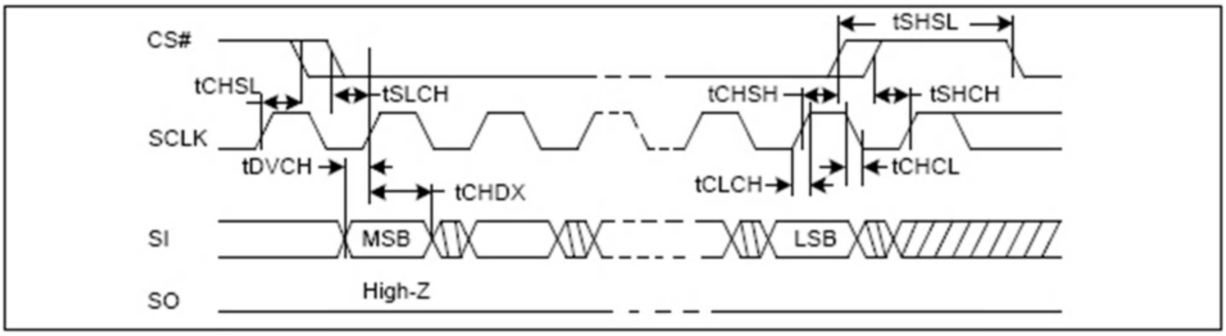


Figure 8-1 Serial Input Timing

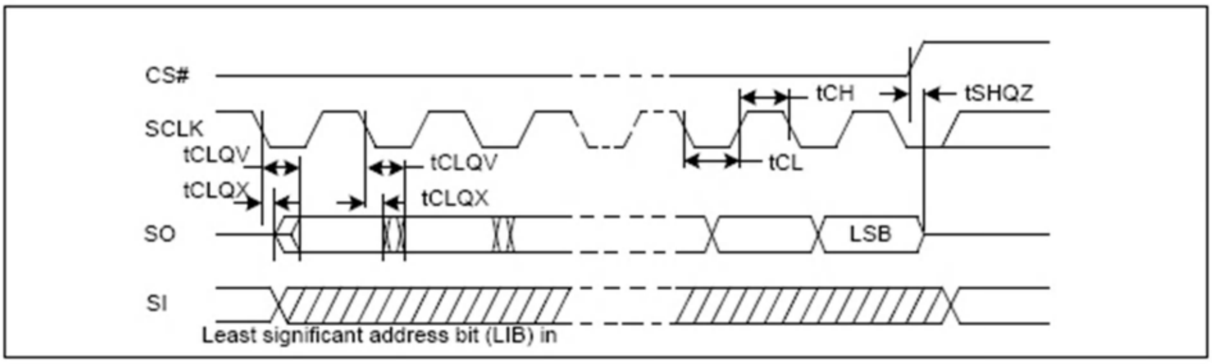


Figure 8-2 Output Timing

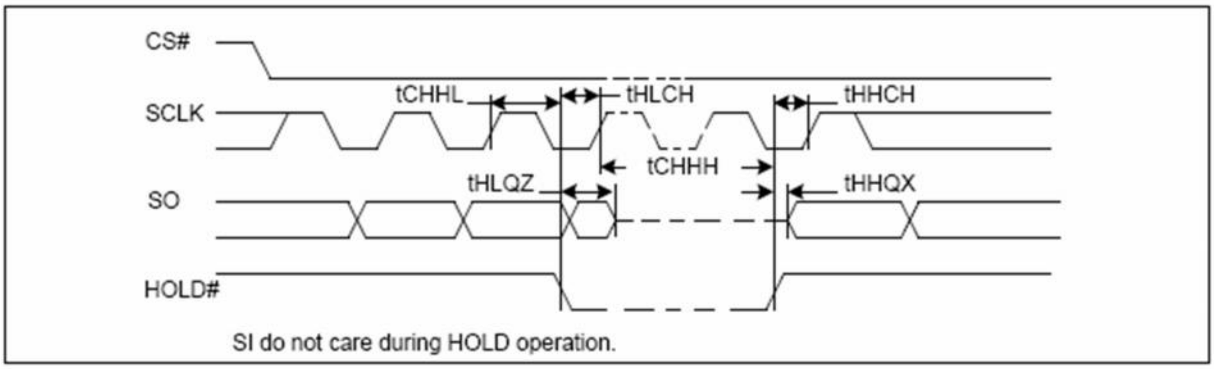
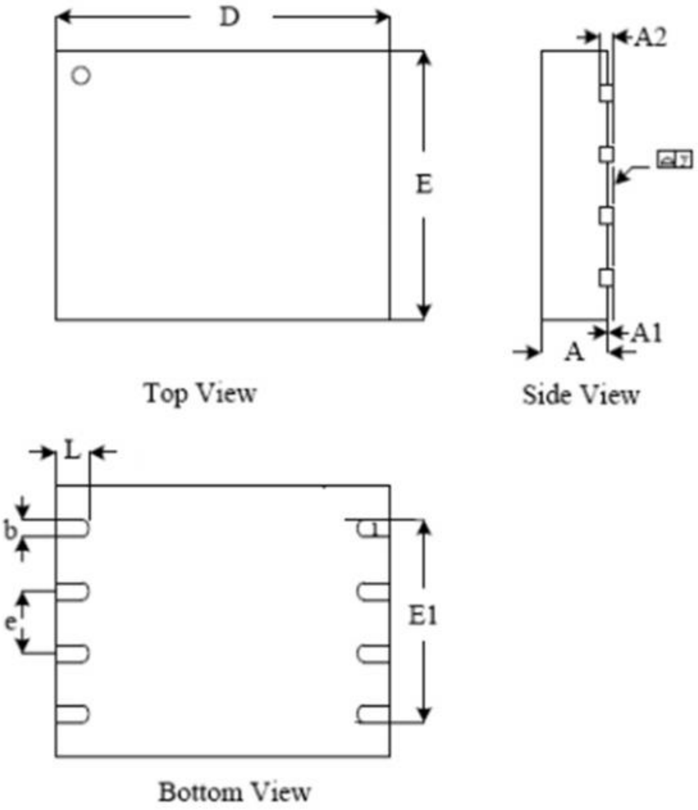


Figure 8-3 Hold Timing

9 Package Outline Information



Symbol / Unit		A	A1	A2	b	D	D1	E	E1	e	y	L
mm	Min	0.78			0.6	7.95	3.25	5.95	4.4		0.00	0.75
	Nom	0.8		0.20	0.65	8.00	3.40	6.00	4.5	1.27		0.8
	Max	0.85	0.05		0.7	8.05	3.50	6.05	4.6		0.05	0.85